The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YUVAL BACHRACH

Appeal No. 2006-1018
Application No. 09/471,637

ON BRIEF

Before THOMAS, KRASS and HOMERE, **Administrative Patent Judges.**

HOMERE, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 21, all of which are pending in this application.

Invention

Appellant's invention relates generally to a word-based interface system (132) with adaptive speed for facilitating communication between the physical layer (PHY) (126) and the medium access control sub-layer (MAC) (124) of the data link layer. The MAC

includes at least one PHY-to-MAC port (134) for receiving signals indicative of words originated from the PHY in destination to the MAC. The MAC also includes a MAC-to-PHY port (136) for transmitting signals indicative of words originated from the MAC in destination to the PHY. The PHY-to MAC words include a slow mode wherein each word received by the MAC from the PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

Claim 1 is representative of the claimed invention and is reproduced as follows:

1. A MAC comprising:

at least one PHY-to-MAC port to receive signals indicative of PHY-to-MAC words; and

at least one MAC-to-PHY port to transmit signals indicative of MAC-to-PHY words;

wherein the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

References

The Examiner relies on the following references:

Boucher et al. (Boucher)	6,427,173	July 30, 2002 Filed on December 15, 1999
Findlater et al. (Findlater)	6,385,208	May 07, 2002 Filed on June 02, 1998
Rubin	4,525,795	June 25, 1985

Rejections At Issue

A. Claims 1, 2, 8, 9 and 15-16 stand rejected under 35 U.S.C. § 102 as being anticipated by Boucher.

B. Claims 3, 4 and 6 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Boucher and Rubin.

C. Claims 5, 7, 10-14 and 17-21 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Boucher and Findlater.

Rather than reiterating the arguments of Appellant and the Examiner, the opinion refers to respective details in the Briefs[1] and the Examiner's Answer.[2] Only those arguments actually made by Appellant have been considered in this decision. Arguments, which Appellant could have made but chose not to make in the Briefs have not been taken into consideration. See 37 CFR 41.37(c)(1) (vii) (eff. Sept. 13, 2004).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the Examiner's rejections, the arguments in support of the rejections and the evidence of anticipation and obviousness relied upon by the Examiner as support for the rejections. We have likewise reviewed and taken into consideration Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in the rebuttal set forth in the Examiner's Answer.

[1] Appellant filed a corrected Appeal Brief on May 03, 2005. Appellant filed a Reply Brief on October 21, 2005. Appellant filed a supplemental Appeal Brief on February 15, 2006.
[2] The Examiner mailed an Examiner's Answer on August 25, 2005. Examiner mailed a communication on January 24, 2006 indicating that the Reply Brief has been entered and considered.

After full consideration of the record before us, we agree with the Appellant that claims 1, 2, 8, 9 and 15-16 are not properly rejected under 35 U.S.C. § 102 as being anticipated by Boucher. We further agree with the Appellant that claims 3, and 10-14 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Boucher and Rubin. Additionally, we agree with the Appellant that claims 5, 7, 10-14 and 17-21 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Boucher and Findlater. Accordingly, we reverse the Examiner's rejections of claims 1-21 for the reasons set forth **infra**.

I. Under 35 U.S.C. § 102(e), is the Rejection of Claims 1, 2, 8, 9 15 and 16 as Being Anticipated By Boucher Proper?

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. **See In re King**, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and **Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.**, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

With respect to the Boucher reference, Appellant argues at page 6 of the Appeal Brief that Boucher does not teach a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the

slow mode PHY-to-MAC word. Appellant further expands on this argument in the Reply Brief. Particularly, at page 2 of the Reply Brief, Appellant states:

> "Specifically, for example as recited in independent claim 1, PHY-to-MAC words include slow mode PHY-to-MAC words received by the MAC layer (e.g., from layer 1 to layer 2) include a transmit cycle field to indicate whether the MAC provides data in a next MAC-to-PHY word from MAC to PHY (e.g., from layer 2 to layer 1). As a result, the speed of packet exchanges between MAC layer and PHY layer can be controlled by both layers via these kinds of communications. It is respectfully submitted that these limitations are absent from Boucher."

Further, at page 3 of the Reply Brief, referring to various sections of Boucher upon which the Examiner relied in the rejection, Appellant states:

> "Although the cited sections mentions (sic) the words of PHY and MAC layers, there is no disclosure or suggestion within Boucher of communications between the PHY layer and the MAC layer using the a transmit cycle field to adapt to various speeds as set forth above."

To determine whether claim 1 is anticipated, we must first determine the scope of the claim. We note that claim 1 reads in part as follows:

> "wherein the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in the a MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word. "

At page 4, lines 22-26, Appellants' specification states:

> "Communication of data across interface 132 is word based. PHY 126 transmits a word to MAC 124 via wires RxD 134 and MAC 124 transmits a word to PHY 126 via wires TxD 136. Words that are transmitted from PHY 126 to MAC 124 are referred to as PtM (PHY-to-MAC)

> words, and words that are transmitted from MAC 124 to PHY 126 are referred to as MtP (MAC-to-PHY) words."

Further, at page 5, lines 13-20, Appellant's specification states:

> "Bit position number 9 in Fig. 2 is the Tx Cyc (Transmit Cycle) field to indicate whether MAC 124 is requested by PHY 126 to send data in the next MtP word. For the particular embodiment of Fig. 2, Tx_Cyc= 1 indicates that PHY 126 is ready for data from MAC 124, whereas Tx_Cyc= 0 indicates that PHY 126 is not ready for data from MAC 124. In this way, various data link speeds may be supported without changing the clock signal frequency on CLK 138. Also, the transmit and receive speeds may be different. Furthermore, even when there is no frame in progress, the Tx_Cyc field may be used by PHY 126 to communicate to MAC 124 the data link speed."

Additionally, at page 6, lines 9-13, Appellant's specification states:

> "For the Slow mode, the data rate at which PHY 126 can transmit on the medium is less than the rate at which MAC 124 can generate data. Consequently the Tx_Cyc field (bit position 9 in Fig. 3) is used in the Slow mode PtM data word because PHY 126 is not always ready to receive data from MAC 124."

Thus, the claim does require a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

Now, the question before us is what Boucher would have taught to one of ordinary skill in the art? To answer this question, we find the following facts:

1. At column 7, line 34- column 8, line 37, Boucher states the following:

> When a message packet or frame is received 47 from a network by the CPD, it is first validated by a hardware assist. This includes determining the protocol types of the various layers, verifying relevant checksums, and

summarizing 57 these findings into a status word or words. Included in these words is an indication whether or not the frame is a candidate for fast-path data flow. Selection 59 of fast-path candidates is based on whether the host may benefit from this message connection being handled by the CPD, which includes determining whether the packet has header bytes indicating particular protocols, such as TCP/IP or SPX/IPX for example. The small percent of frames that are not fast-path candidates are sent 61 to the host protocol stacks for slow-path protocol processing. Subsequent network microprocessor work with each fast-path candidate determines whether a fast-path connection such as a TCP or SPX CCB is already extant for that candidate, or whether that candidate may be used to set up a new fast-path connection, such as for a TTCP/IP transaction. The validation provided by the CPD provides acceleration whether a frame is processed by the fast-path or a slow-path, as only error free, validated frames are processed by the host CPU even for the slow-path processing.

All received message frames which have been determined by the CPD hardware assist to be fast-path candidates are examined 53 by the network microprocessor or INIC comparator circuits to determine whether they match a CCB held by the CPD. Upon confirming such a match, the CPD removes lower layer headers and sends 69 the remaining application data from the frame directly into its final destination in the host using direct memory access (DMA) units of the CPD. This operation may occur immediately upon receipt of a message packet, for example when a TCP connection already exists and destination buffers have been negotiated, or it may first be necessary to process an initial header to acquire a new set of final destination addresses for this transfer. In this latter case, the CPD will queue subsequent message packets while waiting for the destination address, and then DMA the queued application data to that destination.

A fast-path candidate that does not match a CCB may be used to set up a new fast-path connection, by sending 65 the frame to the host for sequential protocol processing. In this case, the host uses this frame to create 51 a CCB, which is then passed to the CPD to control subsequent frames on that connection. The CCB, which is cached 67 in the CPD, includes control and state information pertinent to all protocols that would have been processed had conventional software layer processing been employed. The CCB also contains storage space for per-transfer information used to facilitate moving application-level data contained within subsequent related message packets directly to a host application in a form available for immediate usage. The CPD takes command of connection processing upon receiving a CCB for that connection from the host.

As shown more specifically in FIG. 4A, when a message packet is received from the remote host 22 via network 25, the packet enters hardware receive logic 32 of the CPD 30, which checksums headers and data, and parses the headers, creating a word or words which identify the message packet and status, storing the headers, data and word temporarily in memory 60. As well as validating the packet, the receive logic 32 indicates with the word whether this packet is a candidate for fast-path processing. FIG. 4A depicts the case in which the packet is

not a fast-path candidate, in which case the CPD 30 sends the validated headers and data from memory 60 to data link layer 36 along an internal bus for processing by the host CPU, as shown by arrow 56. The packet is processed by the host protocol stack 44 of data link 36, network 38, transport 40 and session 42 layers, and data (D) 63 from the packet may then be sent to storage 35, as shown by arrow 65.

2. At column 10, lines 19-34, Boucher states the following:

A simplified intelligent network interface card (INIC) 150 is shown in FIG. 6 to provide a network interface for a host 152. Hardware logic 171 of the INIC 150 is connected to a network 155, with a peripheral bus (PCI) 157 connecting the INIC and host. The host 152 in this embodiment has a TCP/IP protocol stack, which provides a slow-path 158 for sequential software processing of message frames received from the network 155. The host 152 protocol stack includes a data link layer 160, network layer 162, a transport layer 164 and an application layer 166, which provides a source or destination 168 for the communication data in the host 152. Other layers which are not shown, such as session and presentation layers, may also be included in the host stack 152, and the source or destination may vary depending upon the nature of the data and may actually be the application layer.

3. At column 26, lines 52-64, Boucher states the following:

Next, a TCP/IP packet is received from the network line 210 via network connector 2101 and Physical Layer Interface (PHY) 2100. PHY 2100 supplies the packet to MAC 402 via a Media Independent Interface (MII) parallel bus 2109. MAC 402 begins processing the packet and asserts a "start of packet" signal on line 2213 indicating that the beginning of a packet is being received. When a byte of data is received in the MAC and is available at the MAC outputs 2215, MAC 402 asserts a "data valid" signal on line 2214. Upon receiving the "data valid" signal, the packet synchronization sequencer 2201 instructs the data synchronization buffer 2200 via load signal line 2222 to load the received byte from data lines 2215.

With the above discussion in mind, we find that Boucher does not teach the invention as claimed. Particularly, we find that Boucher teaches an intelligent network interface card (INIC) that provides a network interface for data communication for a host computer. The INIC determines whether received message packets should be forwarded for past path processing or slow path processing based upon a comparison between the

header information in each data packet and the communication control block (CCB) data. Boucher also teaches that each packet contains words that are received at the Physical link layer, communicated to the MAC layer for processing, and subsequently output to the communication medium. Hence, it is our finding that one of ordinary skill in the art would have duly recognized from Boucher's teachings that the disclosed comparison between the CCB data and the header information in each received packet/word to determine which path the packet should be forwarded to is not equivalent to Appellant's claimed PHY-to-MAC word, which includes a transmit cycle field to in a slow mode PHY-to-MAC. Further, Boucher does not teach a MAC-to-PHY communication, as called for by the claim. Consequently, we find error in the Examiner's stated position, which concludes that Boucher teaches the claimed limitation of a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

Therefore, we will not sustain the Examiner's rejection of claims 1, 2, 8, 9, 15 and 16 under 35 U.S.C. § 102(e).

II. Under 35 USC 103, is the Rejection of Claims 3, 4 and 6 as Being Unpatentable over the combination of Boucher and Rubin Proper?

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of obviousness. **In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). **See also In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of

ordinary skill in the art suggests the claimed subject matter. **In re Fine**, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. **See also Piasecki**, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." **In re Lee**, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

With respect to dependent claims 3, 4 and 6, Appellant argues at page 7of the Appeal Brief that Boucher does not teach a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word. Appellant further argues that Rubin does not cure these deficiencies.

We agree with the Appellant that the combination of Boucher and Rubin does not render the cited claims obvious. As noted in the discussion of claim 1 above, we find that Boucher does not teach a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode

PHY-to-MAC word. We find that the Rubin reference does not teach that limitation either. The Rubin reference is merely relied upon for its teaching of words that are 12 bits wide. Thus, the combination of Boucher and Rubin does not teach a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

After consideration of the record before us, we find that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention as set forth in claims 3, 4 and 6. Accordingly, we will not sustain the Examiner's rejection of claims 3, 4 and 6.

III. Under 35 U.S.C. § 103, is the Rejection of Claims 5, 7, 10-14 and 17-21 as Being Unpatentable over the combination of Boucher and Findlater Proper?

With respect to dependent claims 5, 7, 10-14 and 17-21, Appellant argues at page 8 of the Appeal Brief that Boucher does not teach a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word. Appellant further argues that Findlater does not cure these deficiencies.

We agree with the Appellant that the combination of Boucher and Findlater does not render the cited claims obvious. As noted in the discussion of claim 1 above, we find that Boucher does not teach a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY

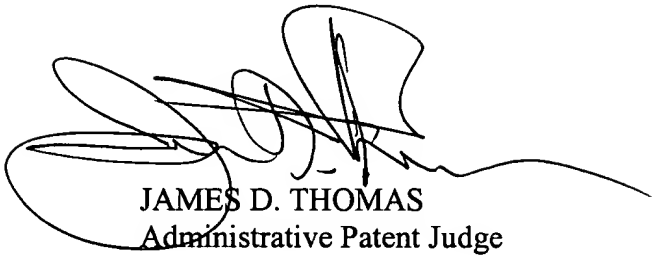
word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word. We find that the Findlater reference does not teach that limitation either. The Findlater reference is merely relied upon for its teaching of PHY-to-MAC words that have data fields in various bit positions. Thus, the combination of Boucher and Findlater does not teach a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

After consideration of the record before us, we find that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention as set forth in claims 5, 7, 10-14 and 17-21. Accordingly, we will not sustain the Examiner's rejection of claims 5, 7, 10-14 and 17-21.

CONCLUSION

In view of the foregoing discussion, we have not sustained the Examiner's decision rejecting claims 1, 2, 8, 9, 15 and 16 under 35 U.S.C. § 102. We have also not sustained the Examiner's decision rejecting claims 3, 4-7, 10-14, and 17-21 under 35 U.S.C. § 103. Therefore, we reverse.

REVERSED



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